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Evidence-Bound Agentic Electrical Engineering

A PCB design sprint as a pre-fabrication qualification case

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Claim boundary. Editable PCB source was generated and checked. Seven routing candidates, 28 engineering discoveries, and 20 append-only evidence events were preserved. No manufacturing release was approved and no physical board was fabricated or tested.

Abstract

General-purpose language models can produce plausible electronic design artifacts, but agreement between a bill of materials, schematic, printed circuit board, and design-rule report does not establish that the represented component or physical mechanism is correct. This paper reports a pre-fabrication case study built around a low-voltage irrigation-controller bench board. The work produced native KiCad source, seven routing candidates, an independent component and assembly contract, deliberate fault mutations, and an append-only evidence archive. A completed route passed native geometry and connectivity checks but was rejected after electrical layout review found an approximately 85.2 mm regulator input-capacitor path and other physically important defects. A later corrected seed exposed a different failure: Freerouting completed internal search under several stopping conditions but did not persist a route-session file. We argue that an agentic electrical engineering system must treat requirements, component identity, CAD geometry, layout intent, tool transactions, manufacturing release, and physical measurement as separate evidence-bearing contracts. The resulting architecture uses an exact-part component intelligence graph, replaceable deterministic tools, independent validators, explicit human authority, and physical feedback. The case does not claim a working or manufacturer-ready PCB.

1 Introduction

Generating a schematic or routing copper is only one part of electrical engineering. A useful system must decide whether the requested operating envelope is complete, whether the exact orderable part matches its symbol and footprint, whether the layout preserves the physical current path, whether the manufacturing outputs come from one reviewed source state, and whether the assembled board behaves as required.

Recent work has shown growing interest in language models for electronic design automation, including HDL generation and analysis [13], constraint-guided PCB schematic synthesis [14], multi-agent analog design [1], and learned PCB placement [6]. These systems make important progress on synthesis and optimization. The case in this paper examines a complementary question: *what evidence and operating machinery are needed before generated PCB artifacts may cross into manufacturing?*

The contribution is not a new autorouter. It is an observed failure map and a system boundary:

1. native EDA agreement is separated from component and physical validity;
2. every design and tool transition produces a hash-bound, inspectable event, including absent outputs;
3. exact component identity binds evidence, pins, CAD, mechanical geometry, manufacturing metadata, rights, and review state;
4. routing, release, external upload, purchase, and physical qualification remain independent capabilities with explicit authority.

2 Case boundary and method

2.1 Reference board

The case uses a 12 V, one-channel bench controller intended to exercise power conversion, current sensing, protected low-side switching, a hard-stop loop, watchdog timing, reset supervision, local control, connectors, test points, and manufacturing exports. The board is deliberately outside a field-qualified product claim. Direct mains, battery charging, radio, safety credit, EMC

compliance, environmental qualification, and agricultural-impact claims are excluded.

Table 1: Evidence boundary at sprint freeze.

Item	Observed evidence	State
Native source	Editable KiCad schematic, PCB, project, symbols, footprints, and 3D assets	Generated
Candidate 7 seed	Zero pre-route placement/copper violations, zero schematic-parity differences, 109 expected unconnected items	Checked seed
Semantic contract	13 critical parts, 57 BOM rows, 49 populated SMD placements, 18 official footprint pad sets	Pass
Fault mutations	Swapped diode, invalid ADC assignment, missing SMD attribute, wrong switch-land coordinate	All rejected
Accepted route	No Candidate 7 route-session file exists	Open
Manufacturing package	Superseded package quarantined and removed from the active export directory	Fabrication stop
Physical board	No order, assembly, power-up, measurement, or field test	Not started

2.2 Tool and evidence model

KiCad 10.0.3 was used for native source, checks, exports, and 3D rendering [5]. Freerouting 2.2.4 was evaluated as a replaceable global routing adapter [3]. The exact KiCad disk image and Freerouting JAR were identified by SHA-256 in the run record. Those hashes identify the tool bytes; they do not qualify the design.

Each meaningful attempt was recorded as an append-only event containing:

- the observed outcome and engineering decision;
- copied source, report, image, route, or log artifacts;
- byte size and SHA-256 for every copied file;
- tool method, source revision, and dirty-worktree state;
- every expected output that was not created.

At freeze, the archive contained 20 events, 216 artifacts, and 41,310,214 bytes. All recorded sizes and hashes verified. A missing route session was represented as a named absence, not an empty file.

The first semantic-verifier rerun after scratch cleanup failed before validation because its default CPL path still pointed into the removed temporary directory. The exact 49-row export was promoted into the durable verification set, checked byte-for-byte against its archived copy, and the semantic and deliberate-fault tests then passed. This raised the discovery count to 28. The incident shows that a passing check is not reproducible evidence unless every input survives the cleanup that follows the run.

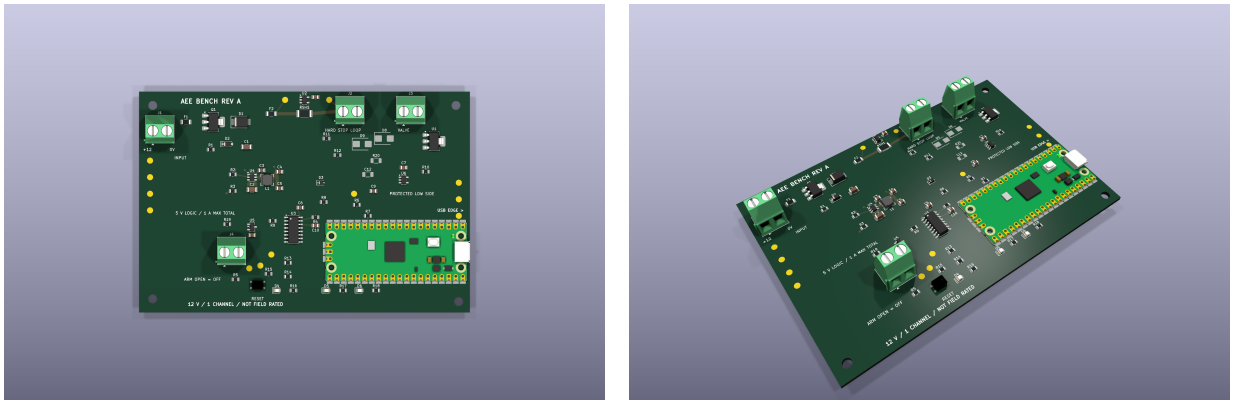


Figure 1: Candidate 7 top and isometric KiCad renders. These are images of the corrected, copper-free qualification seed. They are not photographs of a manufactured board.

3 What failed

3.1 Representation agreement did not establish part correctness

Early checks showed that the schematic and PCB could agree while both were wrong. A tactile switch was initially represented as two large lands even though the physical part uses four terminals with internally common pairs. A first correction then interpreted the terminal numbering around the symmetric package incorrectly. The final mapping required visual comparison of every manufacturer callout and the contact diagram [7].

Other joins failed differently. A footprint-level assembly attribute was missing even though its pads were typed as SMD, which caused the placement export to omit populated parts. A Pico orientation that looked correct in coordinates placed the USB service direction incorrectly until a real 3D model was rendered and inspected [10]. A regulator headline current was insufficient to establish the board rail rating because inductor current, ripple, copper, temperature, and actual load were separate constraints.

These findings motivated an independent semantic contract. The checker reads the board, BOM, placement output, fixed component expectations, and audited library pad sets without importing constants from the design generator. The positive case and deliberate mutations prevent a wrong generator assumption from silently changing both the artifact and its expected answer.

3.2 A clean route was electrically rejected

Candidate 1 completed all declared connections and passed native DRC and schematic parity. Independent copper-path review then found approximately:

- 85.2 mm between the regulator VIN pin and its input capacitor;
- 11.7 mm between regulator ground and input-capacitor ground;
- 8.75 mm from the switch pin to the inductor;
- 19.4 mm from feedback to the output-capacitor node;
- 4.76 mm in the bootstrap path.

The watchdog timing nets also used vias, and the board had inadequate dedicated ground transfer. These properties matter to the physical mechanisms documented for the switching regulator, current-sense amplifier, and watchdog [2, 11, 12]. They were not encoded in the router objective or the generic DRC rules.

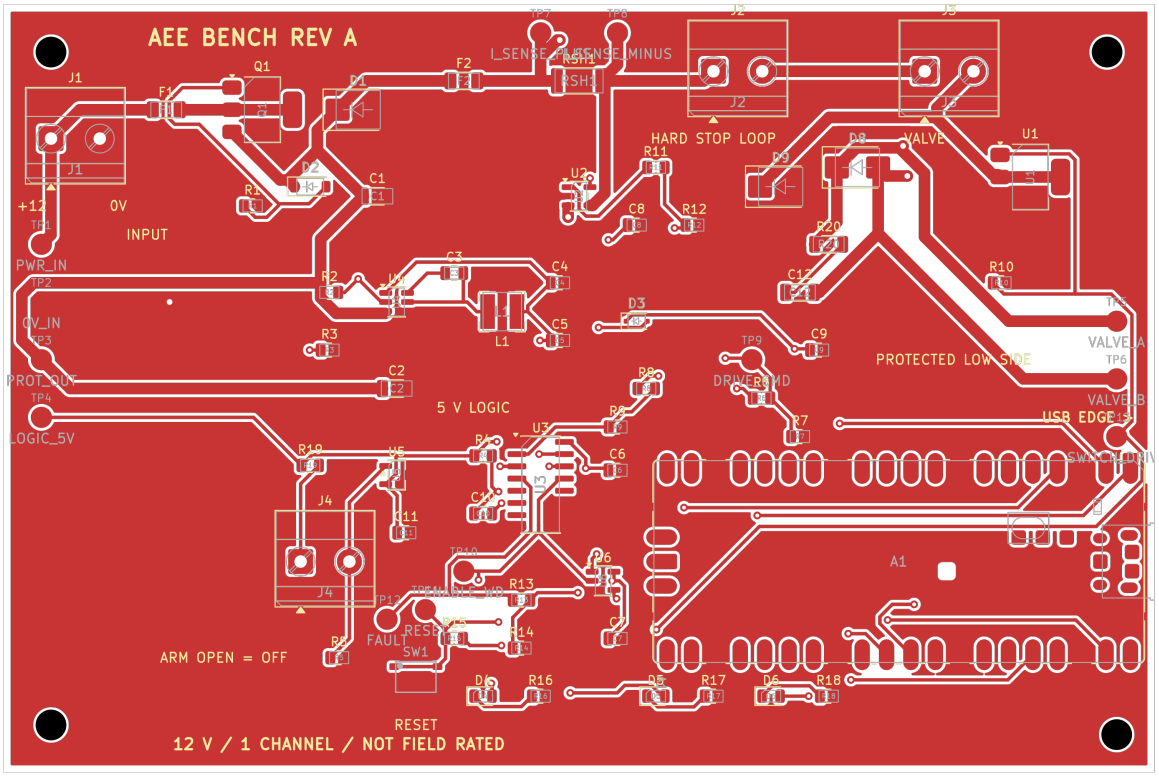


Figure 2: Candidate 1 top-copper review image. The route completed and passed native geometry checks, but was rejected for current-loop geometry and return paths. A red copper plot is not a pass/fail indicator.

3.3 Routing was sensitive to physically useful constraints

Table 2: Routing progression and decision.

Candidate	Observed result	Decision
1	Completed, native checks clean, electrical review failed	Reject geometric completion as fabrication evidence.
2	Fixed critical routes and future ground vias did not complete pass 1	Add plane-stitching vias after routing.
3	Removing future ground vias did not restore convergence	Fixed critical copper still partitioned the search.
4	Ordinary pre-routed critical copper also timed out	Route a copper-free board, then replace controlled nets.
5	Global route stopped quickly with three local opens	Preserve the ordinary-net backbone; rebuild controlled nets.
6	Critical overlay produced crossings, shorts, and open bypasses	Delete imported controlled nets before deterministic reconstruction.
7	Corrected seed; internal search completed under several stop paths but SES persistence repeatedly hung	Freeze as an unrouted qualification fixture and redesign the tool contract.

Candidate 7 separated the clean seed from a router-only DSN. Normal completion, a pseudo-terminal retry, relative output paths, a foreground run, an explicit maximum-pass stop, and a stagnation stop all failed to produce an accepted SES. The final experiment stopped internal routing after 18 passes and 21.43 seconds with 11 bounded local connections open, then was terminated after 90.389 seconds because the save transaction did not complete.

This does not prove that Freerouting generally cannot route the board. It proves that, for this recorded input and environment, an internal completion message was insufficient evidence of a durable output. The reusable contract must check process exit, non-empty output, hash, import, semantic preservation, post-import DRC, and independent current-loop geometry separately.

4 The component intelligence contract

The central object should be one exact orderable MPN and package revision. It must bind facts and assets that conventional file-oriented libraries often leave in separate places:

Table 3: Minimum exact-part evidence package.

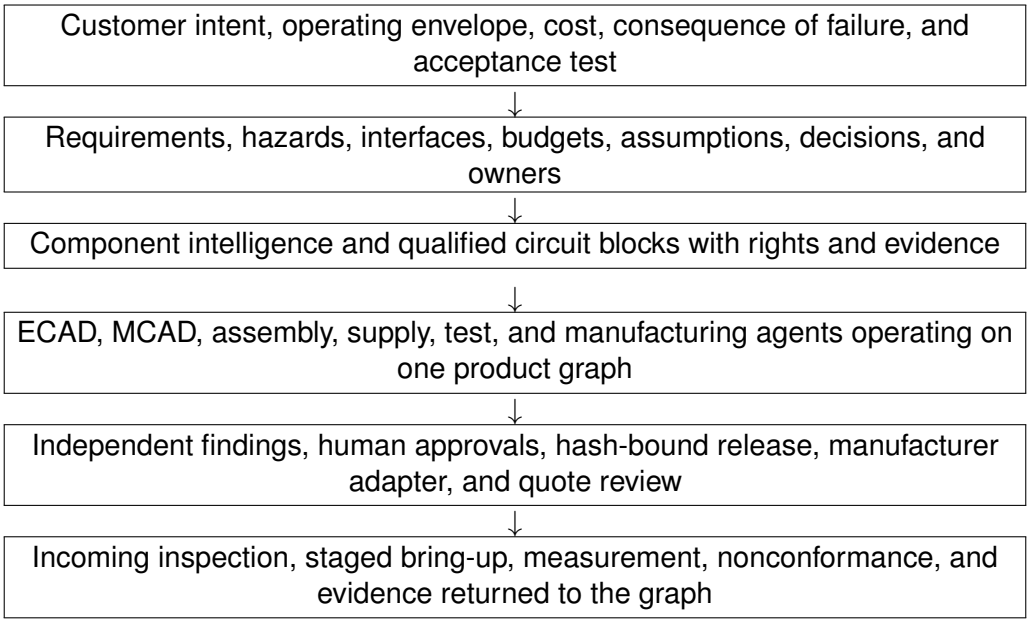
Contract area	Required content
Identity	Manufacturer, exact MPN, ordering suffix, package, temperature grade, revision, and lifecycle state.
Source evidence	Document identity, revision, retrieval date, content hash, exact locator, conditions, exceptions, and rights decision.
Pin semantics	Physical terminal, symbol pin, electrical role, voltage domain, reset state, multiplexing, no-connect, and exposed-pad rules.
CAD assets	Native symbol and footprint, stable identifiers, hashes, tool versions, generated schematic and land-pattern previews.
Mechanical assets	STEP and lightweight model, body envelope, seating plane, origin, axes, pin-one direction, connector and service envelope.
Engineering limits	Absolute maximum, recommended, guaranteed, typical, derived, and measured values retained as different authority classes.
Manufacturing	Mount type, polarity, rotation convention, MSL and process limits where sourced, plus vendor codes as adapter-specific fields.
Validation	Pin/pad comparison, footprint geometry, 3D alignment, mutation tests, review state, known-good project revisions, and physical test scope.

The package also includes symbol, footprint, pinout, top/bottom, and isometric images. These previews allow human and machine vision checks to compare the descriptions before a board is routed.

Rights are part of the schema. A publicly reachable datasheet, STEP file, or vendor symbol is not automatically redistributable. The open library should publish original schemas, normalized facts with an approved basis, lawful CAD assets, generated previews, validators, and measured evidence. Restricted source bytes remain in a local or licensed runtime cache addressed by URL, revision, locator, and hash.

5 System-of-systems architecture

The target is an engineering operating system, not a single PCB agent.



The shared graph holds stable identities for requirements, components, pins, interfaces, assets, findings, waivers, releases, physical units, procedures, and measurements. ECAD contributes nets, pads, keepouts, heat sources, and test access. MCAD contributes bodies, datum, enclosure constraints, fasteners, cable bends, airflow, and service access. Assembly contributes rotations, process limits, inspection points, and rework constraints. Systems engineering owns traceability, configuration, hazards, verification methods, and acceptance.

The orchestrator should remain closed when it contains customer-private data, licensed supplier feeds, vendor credentials, cost history, internal rules, and human review operations. The schemas, neutral adapters, validators, failure corpus, and rights-cleared reference packages can remain open.

6 Manufacturing and operating implications

The stable manufacturing boundary is vendor-neutral: RS-274-X fabrication layers and drills, exact-MPN BOM, metric placements, assembly drawing, notes, and a manifest binding every file hash to one source state. Manufacturer codes, column names, rotations, and API operations belong in explicit adapters, not in the electrical identity model.

Official vendor material reviewed on 13 July 2026 documents approval-gated PCB quotation and ordering APIs for JLCPCB and PCBWay [4, 8]. The reviewed material does not establish a complete, generally available PCBA ordering API at either vendor. PCBWay publishes assembly file requirements for Gerbers, BOM, placement data, and supporting drawings [9]. The first operating workflow should therefore generate and verify a neutral package, then open a human-reviewed upload. Upload, order creation, payment, and tracking remain separate authorities.

A cost-effective engineering service should begin with low-voltage, two- or four-layer control, sensing, and adapter boards using a bounded component catalog and known manufacturing rules. Cost reduction should come from qualified reusable parts and blocks, fixed interviews, independent mutations, standard release packages, and repeatable bring-up. Referral or API revenue is secondary to paid scope, review, first-article test, and managed iteration.

7 Limitations

This case has substantial limits:

- one board class and one local tool environment were studied;
- the product requirements remain incomplete, including the field load, supply, cost target, environment, and acceptance partner;
- the latest generator was archived after changing and has not been rerun to prove reproduction of the frozen board;
- no accepted route or release package exists;
- no SPICE, thermal, EMC, environmental, endurance, or field evidence is reported;
- no physical sample was inspected or measured;
- no claim is made about comparative defect rate, time, or cost against a conventional engineering team;
- no manufacturer partnership or approved API integration exists.

The observations support requirements for a stronger harness. They do not establish that the proposed venture is economically viable or that the method generalizes to RF, high-speed, precision, high-energy, safety-related, or regulated electronics.

8 Next experiment

The next campaign should stop expanding breadth and qualify the 13 critical parts already exercised by the board:

1. revise the component schema around exact-part evidence, previews, STEP alignment, manufacturing metadata, and rights;
2. create independent pin, pad, package, orientation, mount-attribute, and model-alignment tests with deliberate mutations;
3. encode layout intent for switching loops, bootstrap attachment, Kelvin sense, decoupling, returns, creepage, thermal copper, connector access, and rework;
4. make source, component, requirement, design, or tool changes invalidate every dependent export;
5. run KiCad and routing adapters in clean, repeatable environments with explicit input, timeout, exit, output, import, and hash contracts;
6. generate a neutral package and rehearse manufacturer ingestion without purchase;
7. complete independent review, fabricate one low-risk board under owner approval, and return inspection and measurement to the graph;
8. repeat on two materially different boards before making a general capability claim.

Useful metrics are requirement coverage, evidence completeness, mutation detection, review time, release invalidation accuracy, manufacturer-ingestion warnings, first-power-on defects, rework, and the maintenance cost of the component corpus.

9 Conclusion

The sprint did not deliver a physical PCB. It delivered a sharper definition of the system required before one should be ordered.

The main failure was not that an agent could not draw electronics. The main failure was that multiple plausible descriptions could agree while omitting the physical and operational contract

that made the design useful. A clean DRC, zero unconnected items, a matching schematic, a completed router score, and a complete-looking export each answered a narrow question. None answered whether the exact part, current path, release, or physical board was correct.

An end-to-end electrical engineering house should therefore invest first in the component and evidence graph, independent verification, transaction-safe tool adapters, release invalidation, and physical feedback. The orchestrator comes after those modules can state what they know, what they do not know, and why the workflow must stop.

A Reproducibility record

Table 4: Selected immutable identifiers from the sprint.

Item	Identifier
KiCad disk image SHA-256	`065344be912b121e7afd853a21ea29526234830661e1b7a7b7df042163e6cd01`
Freerouting 2.2.4 JAR SHA-256	`f5ed374182900ccc78e473518bbb9f6b869f4a07159495f663a76f52bb10523b`
Candidate 7 PCB SHA-256	`64662e5227b57fdc378b16532d8bc816f65daa8de9466d30fa30d3ebfcd7b6ee`
Candidate 7 schematic SHA-256	`dec7b6874ae0c801bd41b6491f9fe012d98f8d509bf60ae845d2c5ded3661f34`
Candidate 7 top render SHA-256	`cc9f66e6d88b40dc8961804aa4698dbddb79710ebaa44a90fc9eb9b759781797`
Candidate 7 isometric render SHA-256	`3b4bf1b15f56103f74b97f103bbed5938fde64168920b2b24a6eecca1b226c6c`
Archive at freeze	20 events / 216 artifacts / 41,310,214 bytes / zero hash failures

The evidence archive and current generator are not yet released as a standalone public repository. A public artifact package requires a rights review, clean checkout reproduction, removal of internal-only material, and a license decision. The source paper does not rely on a hidden manufactured result.

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