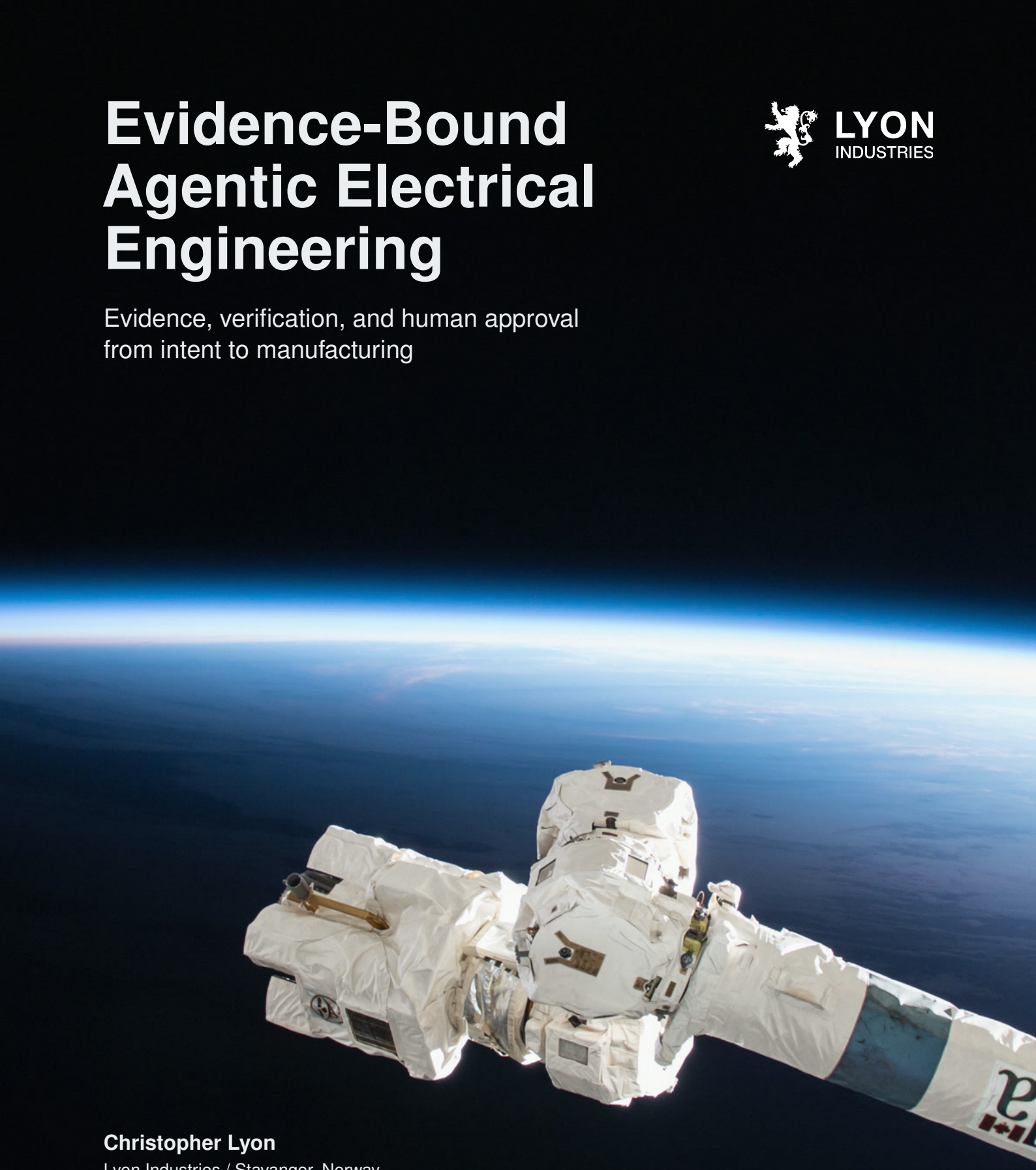
Evidence-Bound Agentic Electrical Engineering

LYON INDUSTRIES

Evidence, verification, and human approval from intent to manufacturing



Christopher Lyon
Lyon Industries / Stavanger, Norway
christopher@lyon-industries.no

PUBLIC REVIEW DRAFT / NOT PEER REVIEWED
Copyright 2026 Lyon Industries. All rights reserved.
lyon-industries.no/white-papers

Cover: Canadarm2 above dark Earth, NASA, 10 September 2015. Public domain.

Abstract

This research programme asks how language-model agents can support electrical engineering from design intent through fabrication and measurement while preserving the evidence required for human approval. This working-paper checkpoint examines a tool-assisted, pre-fabrication case built around a low-voltage irrigation-controller bench board. The work produced native KiCad source, seven non-equivalent routing attempts, a separately implemented component and assembly checker, deliberate fault mutations, and an append-only local archive. The run did not preserve the model version, prompts, tool-call policy, or complete record of human intervention needed to evaluate agent performance. It is therefore reported as an engineering case rather than a model benchmark. KiCad reported zero included violations, zero unconnected items, and zero schematic-parity differences for one completed route under the configured exclusions. Subsequent layout review rejected that route after the archived record reported an approximately 85.2 mm regulator input-capacitor path and other defects. Later Freerouting attempts completed internal search under several stopping conditions without writing a route-session file. These observations motivate proposed requirements for exact-part records, explicit tool-output checks, named human approvals, release invalidation, and physical measurement. Those requirements remain a research plan. This version does not claim a working board, a manufacturer-ready design, or a general agentic engineering capability.

Scope of claims. Editable PCB source was generated and checked. Seven routing candidates, 28 engineering discoveries, and 20 append-only evidence events were preserved. No manufacturing release was approved and no physical board was fabricated or tested.

1 Introduction

The programme's end goal is a traceable workflow from a stated engineering need to a manufactured and measured electrical assembly. The workflow must preserve the source and approval for each decision. This checkpoint asks a narrower question: *what evidence was missing when plausible PCB artifacts were considered for manufacturing?*

Generating a schematic and routing copper answer only part of that question. The requested operating conditions may be incomplete. An orderable part may not match its symbol or footprint. A geometrically legal route may violate the physical current path. Manufacturing files may come from different source revisions. The assembled board may fail even when every digital representation agrees.

Recent work has shown growing interest in language models for electronic design automation, including HDL generation and analysis [16], constraint-guided PCB schematic synthesis [17], multi-agent analog design [1], and learned PCB placement [7]. These systems address synthesis and optimization. This case examines the evidence required before generated PCB artifacts can be approved for manufacturing.

The contribution is a set of observed failure cases and the engineering requirements they motivate:

1. native EDA agreement is separated from component and physical validity;
2. every design and tool transition produces a hash-bound, inspectable event, including absent outputs;
3. exact component identity binds evidence, pins, CAD, mechanical geometry, manufacturing metadata, rights, and review state;
4. routing, release, external upload, purchase, and physical qualification require separate checks and named human approvals.

2 Related work and remaining gap

PCBSchemaGen is the closest published comparison in this review. Its second revision uses a datasheet-derived knowledge graph and a deterministic structural verifier across 227 real-IC tasks [17]. This paper therefore makes no novelty claim for a datasheet knowledge graph, pin-role schema, or structural verifier.

The narrower gap examined here begins after plausible source exists. It covers agreement between EDA files, physical-layout review, external-router process and output state, release invalidation, manufacturer handoff, and evidence returned from a physical article. The current checkpoint observes failures in the first four areas. It proposes later experiments for manufacturer handoff and physical measurement.

Existing manufacturing data standards also constrain that proposal. Ucamco publishes the current Gerber Layer Format and Gerber Job specifications [15]. IPC-2581C defines an intelligent design-to-manufacturing exchange with bidirectional design-for-manufacture feedback [4]. Future work must compare the proposed release record with these established formats rather than inventing a parallel format without a measured need.

3 Case definition and method

3.1 Study provenance and method limits

This checkpoint was assembled from an exploratory design sprint. General-purpose coding agents helped generate and revise source files, scripts, and written records. The sprint did not preserve the exact model identifier, prompts, tool-call permissions, or a complete timeline of human corrections. The paper cannot attribute the observed results to a particular model or compare agent performance with conventional engineering.

The seven routing attempts were adaptive. Each attempt changed in response to the previous result, and the inputs and stopping conditions were not held constant. They are evidence of the recorded tool and workflow failures. They are not controlled comparisons of routing methods. Human review selected the engineering findings. The semantic checker was implemented separately from the design generator, but it was not produced by an independent research group.

3.2 Reference board

The case uses a 12 V, one-channel bench controller intended to exercise power conversion, current sensing, protected low-side switching, a hard-stop loop, watchdog timing, reset supervision, local control, connectors, test points, and manufacturing exports. The board is deliberately outside a field-qualified product claim. Direct mains, battery charging, radio, safety credit, EMC compliance, environmental qualification, and agricultural-impact claims are excluded.

Table 1: Evidence available at sprint freeze.

Item	Observed evidence	State
Native source	Editable KiCad schematic, PCB, project, symbols, footprints, and 3D assets	Generated
Candidate 7 seed	Zero pre-route placement/copper violations, zero schematic-parity differences, 109 expected unconnected items	Checked seed
Semantic checker	13 critical parts, 57 BOM rows, 49 populated SMD placements, 18 official footprint pad sets	Pass
Fault mutations	Swapped diode, invalid ADC assignment, missing SMD attribute, wrong switch-land coordinate	All rejected
Accepted route	No Candidate 7 route-session file exists	Open
Manufacturing package	Superseded package quarantined and removed from the active export directory	Fabrication stop
Physical board	No order, assembly, power-up, measurement, or field test	Not started

3.3 Tool and evidence model

KiCad 10.0.3 was used for native source, checks, exports, and 3D rendering [6]. Freerouting 2.2.4 was evaluated as a replaceable global routing adapter [3]. The exact KiCad disk image and Freerouting JAR were identified by SHA-256 in the run record. Those hashes identify the tool bytes; they do not qualify the design.

The Candidate 1 KiCad report included error, warning, and exclusion severities, but listed five ignored checks: missing courtyards, track endpoints not centred on vias, tuning-profile track geometry, footprint-filter mismatches, and footprint-type mismatches. The result is reported here as zero included DRC findings under the configured exclusions, not as a complete design check.

Each meaningful attempt was recorded as an append-only event containing:

- the observed outcome and engineering decision;
- copied source, report, image, route, or log artifacts;
- byte size and SHA-256 for every copied file;
- tool method, source revision, and dirty-worktree state;
- every expected output that was not created.

At freeze, the archive contained 20 events, 216 artifacts, and 41,310,214 bytes. All recorded sizes and hashes verified. A missing route session was represented as a named absence, not an empty file.

The first semantic-verifier rerun after scratch cleanup failed before validation because its default CPL path still pointed into the removed temporary directory. The exact 49-row export was promoted into the durable verification set, checked byte-for-byte against its archived copy, and the semantic and deliberate-fault tests

then passed. This raised the discovery count to 28. The incident shows that a passing check is not reproducible evidence unless every input survives the cleanup that follows the run.

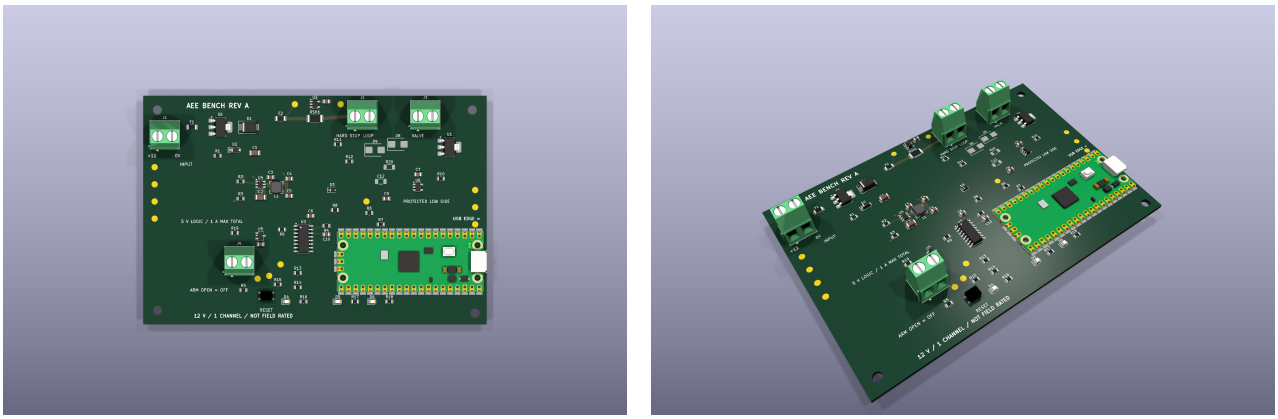


Figure 1: Candidate 7 top and isometric KiCad renders. These are images of the corrected, copper-free qualification seed. They are not photographs of a manufactured board.

4 What failed

4.1 Representation agreement did not establish part correctness

Early checks showed that the schematic and PCB could agree while both were wrong. A tactile switch was initially represented as two large lands even though the physical part uses four terminals with internally common pairs. A first correction then interpreted the terminal numbering around the symmetric package incorrectly. The final mapping required visual comparison of every manufacturer callout and the contact diagram [8].

Other joins failed differently. A footprint-level assembly attribute was missing even though its pads were typed as SMD, which caused the placement export to omit populated parts. A Pico orientation that looked correct in coordinates placed the USB service direction incorrectly until a real 3D model was rendered and inspected [12]. A regulator headline current was insufficient to establish the board rail rating because inductor current, ripple, copper, temperature, and actual load were separate constraints.

These findings motivated a separately implemented semantic checker. It reads the board, BOM, placement output, fixed component expectations, and audited library pad sets without importing constants from the design generator. The positive case and deliberate mutations prevent a wrong generator assumption from silently changing both the artifact and its expected answer.

4.2 A route with zero included DRC findings was rejected

Candidate 1 completed all declared connections. KiCad reported zero included DRC findings, zero unconnected items, and zero schematic-parity differences under the configured exclusions. Subsequent copper-path review recorded these approximate values:

- 85.2 mm between the regulator VIN pin and its input capacitor;
- 11.7 mm between regulator ground and input-capacitor ground;
- 8.75 mm from the switch pin to the inductor;
- 19.4 mm from feedback to the output-capacitor node;
- 4.76 mm in the bootstrap path.

The sprint preserved these values in the engineering record but did not preserve a reusable measurement script, endpoint table, or annotated output. They are diagnostic observations in this checkpoint. A later revision must publish the measurement method and reproduce the values before treating them as repeatable quantitative results.

The watchdog timing nets also used vias, and the board had inadequate dedicated ground transfer. These properties matter to the physical mechanisms documented for the switching regulator, current-sense amplifier, and watchdog [2, 13, 14]. They were not encoded in the router objective or the generic DRC rules.

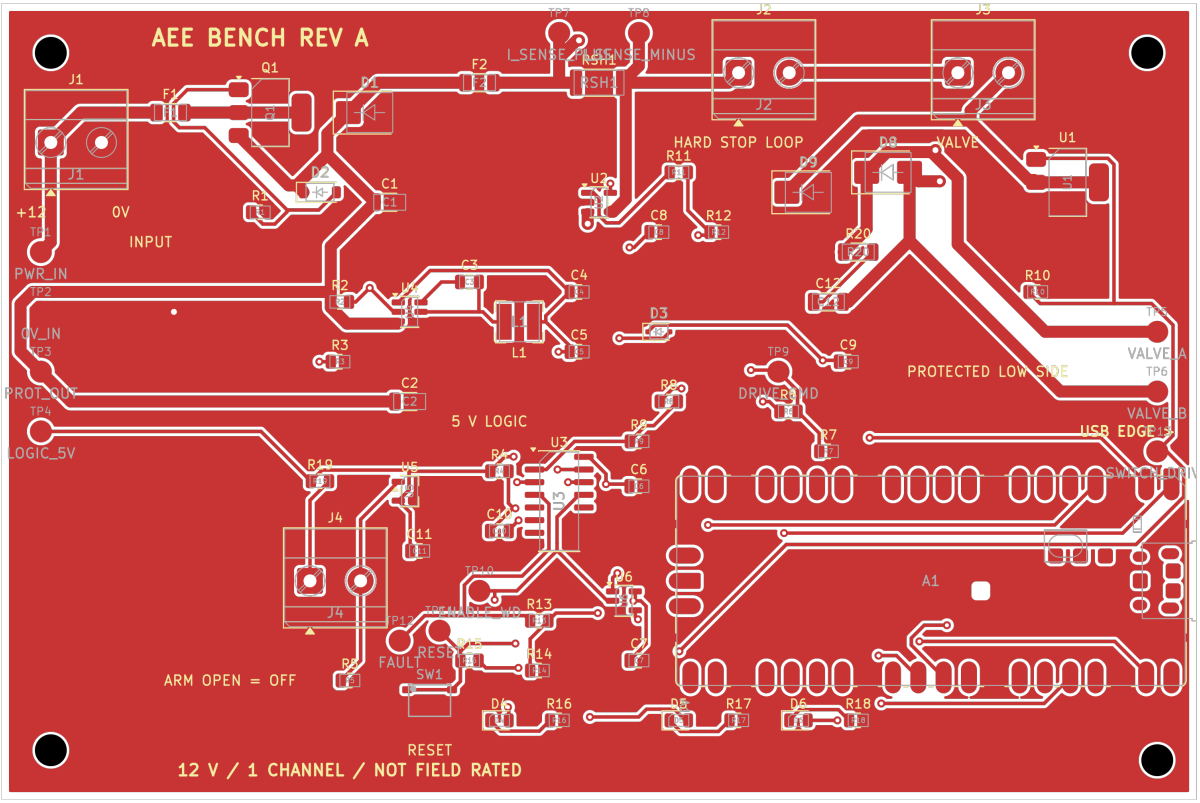


Figure 2: Candidate 1 top-copper review image. KiCad reported zero included DRC findings under the configured exclusions. Subsequent review rejected the current-path geometry and returns. The measurement endpoints are not annotated in this checkpoint.

4.3 Observed outcomes from seven non-equivalent routing attempts

Table 2: Adaptive routing attempts and resulting decisions.

Candidate	Observed result	Decision
1	Completed, zero included DRC findings, layout review failed	Reject geometric completion as fabrication evidence.
2	Fixed critical routes and future ground vias did not complete pass 1	Add plane-stitching vias after routing.
3	Removing future ground vias did not restore convergence	Fixed critical copper still partitioned the search.
4	Ordinary pre-routed critical copper also timed out	Route a copper-free board, then replace controlled nets.
5	Global route stopped quickly with three local opens	Preserve the ordinary-net backbone; rebuild controlled nets.
6	Critical overlay produced crossings, shorts, and open bypasses	Delete imported controlled nets before deterministic reconstruction.
7	Corrected seed; internal search completed under several stop paths but SES persistence repeatedly hung	Freeze as an unrouted qualification fixture and redesign the tool adapter.

Candidate 7 separated the clean seed from a router-only DSN. Normal completion, a pseudo-terminal retry, relative output paths, a foreground run, an explicit maximum-pass stop, and a stagnation stop all failed to produce an accepted SES. The final experiment stopped internal routing after 18 passes and 21.43 seconds with 11 bounded local connections open, then was terminated after 90.389 seconds because the save transaction did not complete.

For this recorded input and environment, an internal completion message did not establish that a durable output existed. No conclusion about Freerouting's general ability follows from these adaptive trials. A future tool adapter must check process exit, non-empty output, hash, import, semantic preservation, post-import DRC, and a separately implemented current-path review.

5 Proposed exact-part record schema

The proposed schema uses one exact orderable MPN and package revision as its central record. It links facts and assets that file-oriented libraries often store separately:

Table 3: Minimum exact-part evidence package.

Record area	Required content
Identity	Manufacturer, exact MPN, ordering suffix, package, temperature grade, revision, and lifecycle state.
Source evidence	Document identity, revision, retrieval date, content hash, exact locator, conditions, exceptions, and rights decision.
Pin semantics	Physical terminal, symbol pin, electrical role, voltage domain, reset state, multiplexing, no-connect, and exposed-pad rules.
CAD assets	Native symbol and footprint, stable identifiers, hashes, tool versions, generated schematic and land-pattern previews.
Mechanical assets	STEP and lightweight model, body envelope, seating plane, origin, axes, pin-one direction, connector and service envelope.
Engineering limits	Absolute maximum, recommended, guaranteed, typical, derived, and measured values retained as different evidence classes.
Manufacturing	Mount type, polarity, rotation convention, MSL and process limits where sourced, plus vendor codes as adapter-specific fields.
Validation	Pin/pad comparison, footprint geometry, 3D alignment, mutation tests, review state, known-good project revisions, and physical test scope.

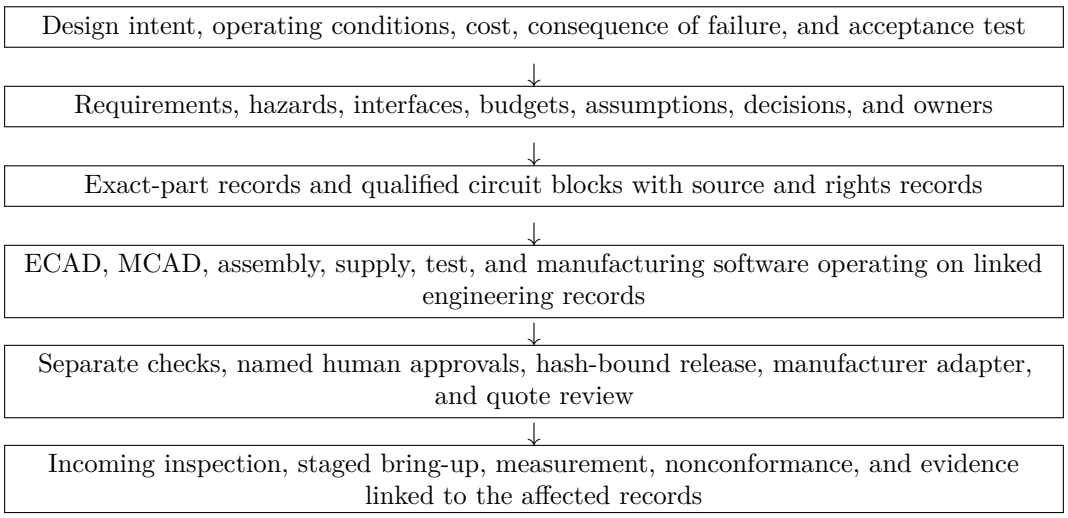
A public implementation now exercises part of this schema [9]. At the cited revision, its catalog contains 20 exact-MPN records under a Draft 2020-12 JSON Schema. The semantic validator passes catalog coverage, identity and path consistency, pin uniqueness, terminal groups, source references, asset paths, orderability, and release state. The AP63205WU-7 regulator and PTS815SJM250SMTRLFS switch from this case are cross-checked; the other 18 records are source-extracted. All remain reference-only and not physically tested.

The target schema also requires native symbols and footprints, pinout, top/bottom and isometric previews, and reviewed STEP models. The public seed contains original symbol and footprint previews for its two cross-checked parts, but it does not distribute production EDA assets or qualified STEP models. Those assets must remain visibly absent until their geometry, provenance, and manufacturing use are reviewed.

Rights are part of the schema. A publicly reachable datasheet, STEP file, or vendor symbol is not automatically redistributable. The public catalog applies this rule to its normalized records and original previews. A complete open library should publish original schemas, normalized facts with an approved basis, lawful CAD assets, generated previews, validators, and measured evidence. Restricted source bytes remain in a local or licensed runtime cache addressed by URL, revision, locator, and hash.

6 Proposed target system

The following architecture is a research hypothesis. It has not been implemented or evaluated end to end.



Proposed target system; not evaluated in this checkpoint.

The proposed shared data model holds stable identities for requirements, components, pins, interfaces, assets, findings, waivers, releases, physical units, procedures, and measurements. ECAD contributes nets, pads, keepouts, heat sources, and test access. MCAD contributes bodies, datum, enclosure constraints, fasteners, cable bends, airflow, and service access. Assembly contributes rotations, process limits, inspection points, and rework constraints. Systems engineering owns traceability, configuration, hazards, verification methods, and acceptance.

A deployed coordinating service would need to protect customer data, licensed supplier feeds, vendor credentials, cost history, internal rules, and human review records. Schemas, neutral adapters, validators, failure cases, and rights-cleared reference packages can be published when their provenance and licenses permit it.

7 Manufacturing and operating implications

A proposed manufacturer handoff contains fabrication layers and drills, exact-MPN BOM, metric placements, assembly drawing, notes, and a manifest that binds each file hash to one source revision. The format choice remains open. Current Gerber specifications support layer and job data, while IPC-2581C defines a broader intelligent exchange [15, 4]. Manufacturer codes, column names, rotations, and API operations belong in named vendor transforms rather than the electrical part record.

Official vendor material reviewed on 13 July 2026 documents approval-gated PCB quotation and ordering APIs for JLCPCB and PCBWay [5, 10]. The reviewed material does not establish a complete, generally available PCBA ordering API at either vendor. PCBWay publishes assembly file requirements for Gerbers, BOM, placement data, and recommends supporting drawings [11]. The first operating workflow should therefore generate and verify a neutral package, then open a human-reviewed upload. Upload, order creation, payment, and tracking require separate actions and approvals.

An initial operational study should use low-voltage, two- or four-layer control, sensing, and adapter boards with a fixed component set and documented manufacturing rules. It should measure engineering hours, review effort, component-data maintenance, tool cost, fabrication cost, first-article defects, and rework. This checkpoint makes no claim of lower cost or commercial value.

8 Limitations

This case has substantial limits:

- the model identifier, prompts, tool-call policy, and complete record of human intervention were not preserved;
- one board class and one local tool environment were studied;
- the seven routing attempts were adaptive and non-equivalent, with no repeated trials, alternative router, or conventional-engineer baseline;
- the reported KiCad result excluded five check categories;
- the path-length record has no published measurement script, endpoint table, uncertainty analysis, or annotated figure;
- the author performed the engineering and review; no independent technical reviewer has signed the findings;

- the product requirements remain incomplete, including the field load, supply, cost target, environment, and acceptance partner;
- the latest generator was archived after changing and has not been rerun to prove reproduction of the frozen board;
- no accepted route or release package exists;
- no SPICE, thermal, EMC, environmental, endurance, or field evidence is reported;
- no physical sample was inspected or measured;
- the public component catalog contains validated reference records, not production-approved EDA assets; only two of this board's 13 critical MPNs are present, and none is physically verified;
- no claim is made about comparative defect rate, time, or cost against a conventional engineering team;
- no manufacturer partnership or approved API integration exists.

The observations motivate the proposed checks and future experiments. They do not establish economic viability or generalization to RF, high-speed, precision, high-energy, safety-related, or regulated electronics.

9 Next experiments and deliverables

The next campaign should strengthen the method and qualify the 13 critical parts already exercised by the board:

1. record the model identifier, prompts or prompt hashes, tool permissions, human instructions and edits, environment, stopping rules, and artifact selection while the work runs;
2. publish a rights-cleared evidence supplement and reproduce the frozen source from a clean checkout;
3. implement and publish the copper-path measurement method, endpoint table, raw output, and annotated rejected-route figure;
4. add the remaining 11 critical exact MPNs to the public component catalog, then add native symbols, footprints, and STEP models only after geometry, provenance, and rights review;
5. create separately implemented pin, pad, package, orientation, mount-attribute, and model-alignment tests with deliberate mutations;
6. encode layout intent for switching loops, bootstrap attachment, Kelvin sense, decoupling, returns, creepage, thermal copper, connector access, and rework;
7. make source, component, requirement, design, or tool changes invalidate every dependent export;
8. run KiCad and at least two routing adapters in clean, repeatable environments with controlled inputs, repeated trials, and explicit input, timeout, exit, output, import, and hash checks;
9. generate a neutral package and rehearse manufacturer ingestion without purchase;
10. complete independent review, fabricate one low-risk board under owner approval, and link inspection and measurement to the affected records;
11. repeat on two materially different boards before making a general capability claim.

Useful metrics are requirement coverage, evidence completeness, mutation detection, review time, release invalidation accuracy, manufacturer-ingestion warnings, first-power-on defects, rework, and the maintenance cost of the component corpus. Agent evaluation also requires intervention count, accepted and rejected changes, time by task, and a conventional engineering baseline.

10 Conclusion

This checkpoint produced no physical PCB. It preserved a set of failures that define the next research work. Candidate 1 showed that zero included DRC findings and complete represented connectivity can coexist with a rejected physical layout. Candidate 7 showed that internal router completion can occur without a durable output file. The component audit showed that agreement between generated files can preserve the same wrong part assumption.

These observations justify testing exact-part records, separately implemented checks, explicit tool-output transactions, release invalidation, named human approvals, and measurements from fabricated boards. The public component catalog is the first partial implementation. Its records remain reference-only.

The programme's end goal remains a traceable workflow from intent to a manufactured and measured assembly. Future revisions will replace the proposed requirements with controlled results, physical measurements, cost evidence, or documented rejection.

A Local artifact-integrity record

Table 4: Selected immutable identifiers from the sprint.

Item	Identifier
KiCad disk image SHA-256	`065344be912b121e7afd853a21ea29526234830661e1b7a7b7df042163e6cd01`
Freerouting 2.2.4 JAR SHA-256	`f5ed374182900ccc78e473518bbb9f6b869f4a07159495f663a76f52bb10523b`
Candidate 7 PCB SHA-256	`64662e5227b57fdc378b16532d8bc816f65daa8de9466d30fa30d3ebfcd7b6ee`
Candidate 7 schematic SHA-256	`dec7b6874ae0c801bd41b6491f9fe012d98f8d509bf60ae845d2c5ded3661f34`
Candidate 7 top render SHA-256	`cc9f66e6d88b40dc8961804aa4698dbddb79710ebaa44a90fc9eb9b759781797`
Candidate 7 isometric render SHA-256	`3b4bf1b15f56103f74b97f103bbed5938fde64168920b2b24a6eecca1b226c6c`
Archive at freeze	20 events / 216 artifacts / 41,310,214 bytes / zero hash failures

The evidence archive and current generator are not yet released as a standalone public repository. The hashes above establish local identity and integrity; they do not establish independent reproduction. A public artifact package requires a rights review, clean-checkout reproduction, removal of internal-only material, and a license decision. This paper does not rely on an undisclosed manufactured result.

Data availability and disclosure

The component records cited in the exact-part schema section are public at the commit listed in the bibliography. The full design archive remains local for the reasons above. The author owns Lyon Industries and the component-catalog repository and is evaluating a possible engineering service based on this research. This paper reports no customer, manufacturer partnership, commercial traction, or comparative cost advantage.

References

[1] Zhixuan Bao, Zhuoyi Lin, Jiageng Wang, Jinhai Hu, Yuan Gao, Yaoxin Wu, Xiaoli Li, and Xun Xu. AnalogAgent: Self-improving analog circuit design automation with LLM agents, 2026. URL: https://arxiv.org/abs/2603.23910, arXiv:2603.23910.

[2] Diodes Incorporated. *AP63205 Datasheet*, 2024. Manufacturer datasheet; accessed 13 July 2026. URL: https://www.diodes.com/datasheet/download/AP63200-AP63201-AP63203-AP63205.pdf.

[3] Freerouting contributors. Freerouting 2.2.4, 2026. Release used in the case study; accessed 13 July 2026. URL: https://github.com/freerouting/freerouting/releases/tag/v2.2.4.

[4] IPC International. IPC-2581C: Generic requirements for printed board assembly products manufacturing description data and transfer methodology, 2020. Official revision announcement, 1 December 2020; accessed 13 July 2026. URL: https://www.electronics.org/news-release/ipc-releases-ipc-2581-revision-c-generic-requirements-printed-board-assembly-products.

[5] JLCPCB. JLCPCB online API access application, 2026. Accessed 13 July 2026. URL: https://jlcpcb.com/help/article/jlcpcb-online-api-available-now.

[6] KiCad Developers Team. *KiCad 10.0 Command-Line Interface Documentation*, 2026. Accessed 13 July 2026. URL: https://docs.kicad.org/10.0/en/cli/cli.html.

[7] Kart Leong Lim. Component centric placement using deep reinforcement learning, 2026. URL: https://arxiv.org/abs/2602.23540, arXiv:2602.23540.

[8] Littelfuse and C&K. *PTS815 Series Tactile Switch Datasheet*, 2026. Manufacturer drawing reviewed 13 July 2026. URL: https://www.littelfuse.com/assetdocs/littelfuse-c-k-tactile-pts815-series-datasheet?assetguid=1c4ee7c5-01fd-4370-a5cc-03ec62685e73.

[9] Lyon Industries. Component intelligence: Evidence-bound component records, 2026. Public catalog at commit 64c14e33be7fff137449621176e2894cc6a65e57; accessed 13 July 2026. URL: https://github.com/lyon-industries/component-intelligence/tree/64c14e33be7fff137449621176e2894cc6a65e57.

[10] PCBWay. API cooperation, 2026. Accessed 13 July 2026. URL: https://www.pcbway.com/api_cooperation.html.

[11] PCBWay. PCB assembly file requirements, 2026. Accessed 13 July 2026. URL: https://www.pcbway.com/assembly-file-requirements.html.

[12] Raspberry Pi Ltd. *Raspberry Pi Pico Datasheet*, 2025. Manufacturer datasheet; accessed 13 July 2026. URL: https://datasheets.raspberrypi.com/pico/pico-datasheet.pdf.

[13] Texas Instruments. *INA180, INA2180, INA4180 Current-Sense Amplifiers Datasheet*, 2022. Revision H, 19 July 2022; accessed 13 July 2026. URL: https://www.ti.com/lit/ds/symlink/ina180.pdf.

[14] Texas Instruments. *SN54AHCT123A/SN74AHCT123A Dual Retriggerable Monostable Multivibrators Datasheet*, 2025. Revision H, 13 January 2025; accessed 13 July 2026. URL: https://www.ti.com/lit/ds/symlink/sn74ahct123a.pdf.

[15] Ucamco. Gerber layer format and gerber job specifications, 2026. Current specification index reviewed 13 July 2026. URL: https://www.ucamco.com/en/gerber/downloads.

[16] Ruizhe Zhong, Xingbo Du, Shixiong Kai, Zhentao Tang, Siyuan Xu, Hui-Ling Zhen, Jianye Hao, Qiang Xu, Mingxuan Yuan, and Junchi Yan. LLM4EDA: Emerging progress in large language models for electronic design automation, 2024. URL: https://arxiv.org/abs/2401.12224, arXiv:2401.12224.

[17] Huanghaohe Zou, Peng Han, Emad Nazerian, Mafu Zhang, Zhicheng Guo, and Alex Q. Huang. PCBSchemaGen: Reward-guided LLM code synthesis for printed circuit boards (PCB) schematic design with structured verification, 2026. Version 2, revised 17 June 2026; accessed 13 July 2026. URL: https://arxiv.org/abs/2602.00510v2, arXiv:2602.00510.